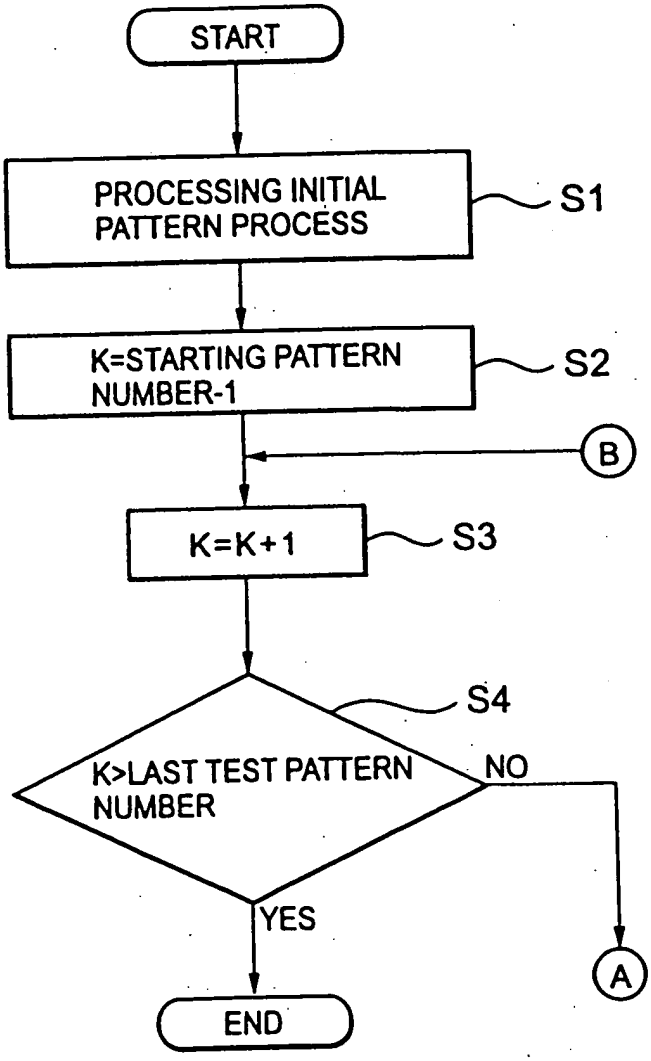
START
PROCESSING INITIAL PATTERN PROCESS
S1
K=STARTING PATTERN NUMBER-1
S2
B
K=K+1
S3
S4
K>LAST TEST PATTERN NUMBER
NO
YES
A
END

FIG.1

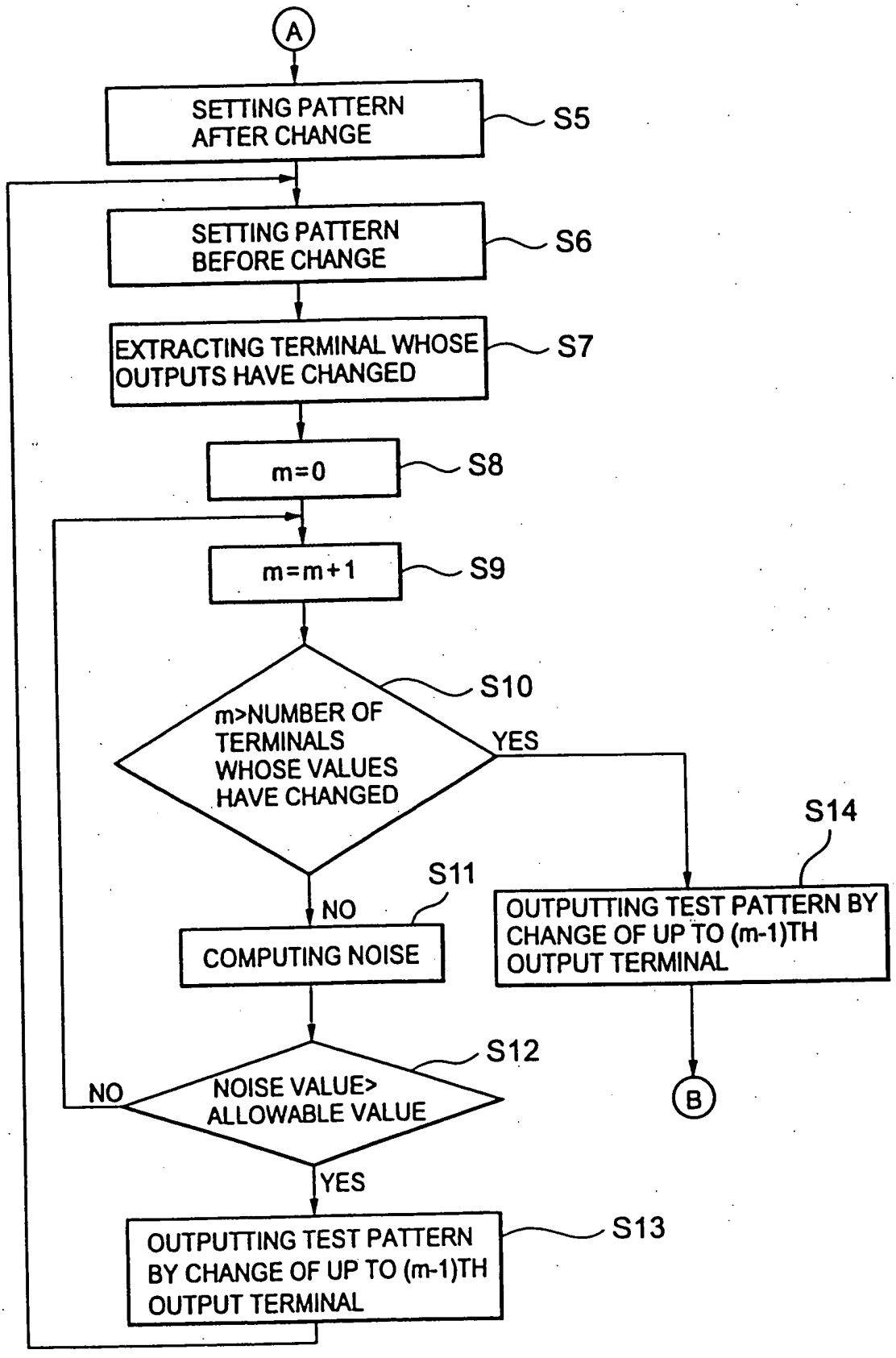
A
SETTING PATTERN AFTER CHANGE
S5
SETTING PATTERN BEFORE CHANGE
S6
EXTRACTING TERMINAL WHOSE OUTPUTS HAVE CHANGED
S7
m=0
S8
m=m+1
S9
m>NUMBER OF TERMINALS WHOSE VALUES HAVE CHANGED
S10
YES
NO
S11
COMPUTING NOISE
NOISE VALUE> ALLOWABLE VALUE
S12
NO
YES
OUTPUTTING TEST PATTERN BY CHANGE OF UP TO (m-1)TH OUTPUT TERMINAL
S13
OUTPUTTING TEST PATTERN BY CHANGE OF UP TO (m-1)TH OUTPUT TERMINAL
S14
B

FIG.2

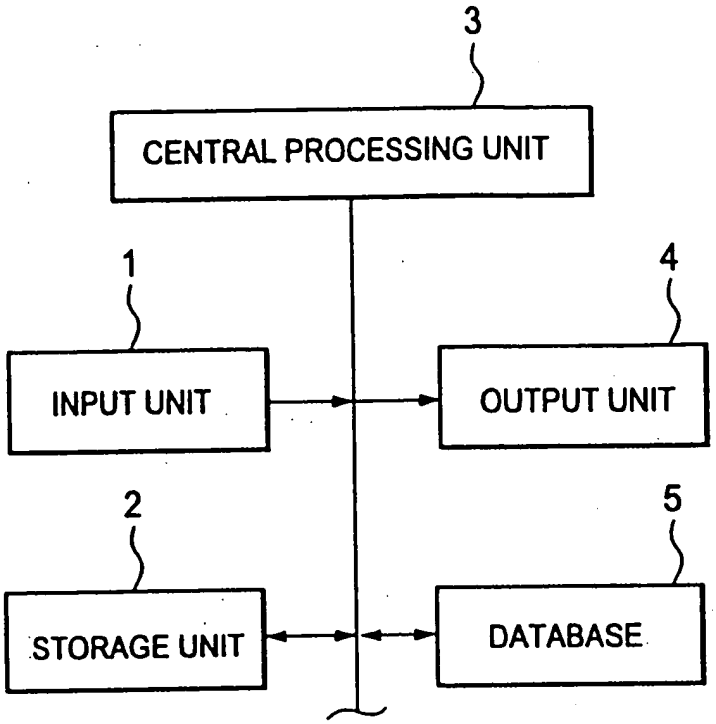
3
CENTRAL PROCESSING UNIT
1
INPUT UNIT
4
OUTPUT UNIT
2
STORAGE UNIT
5
DATABASE

FIG.3

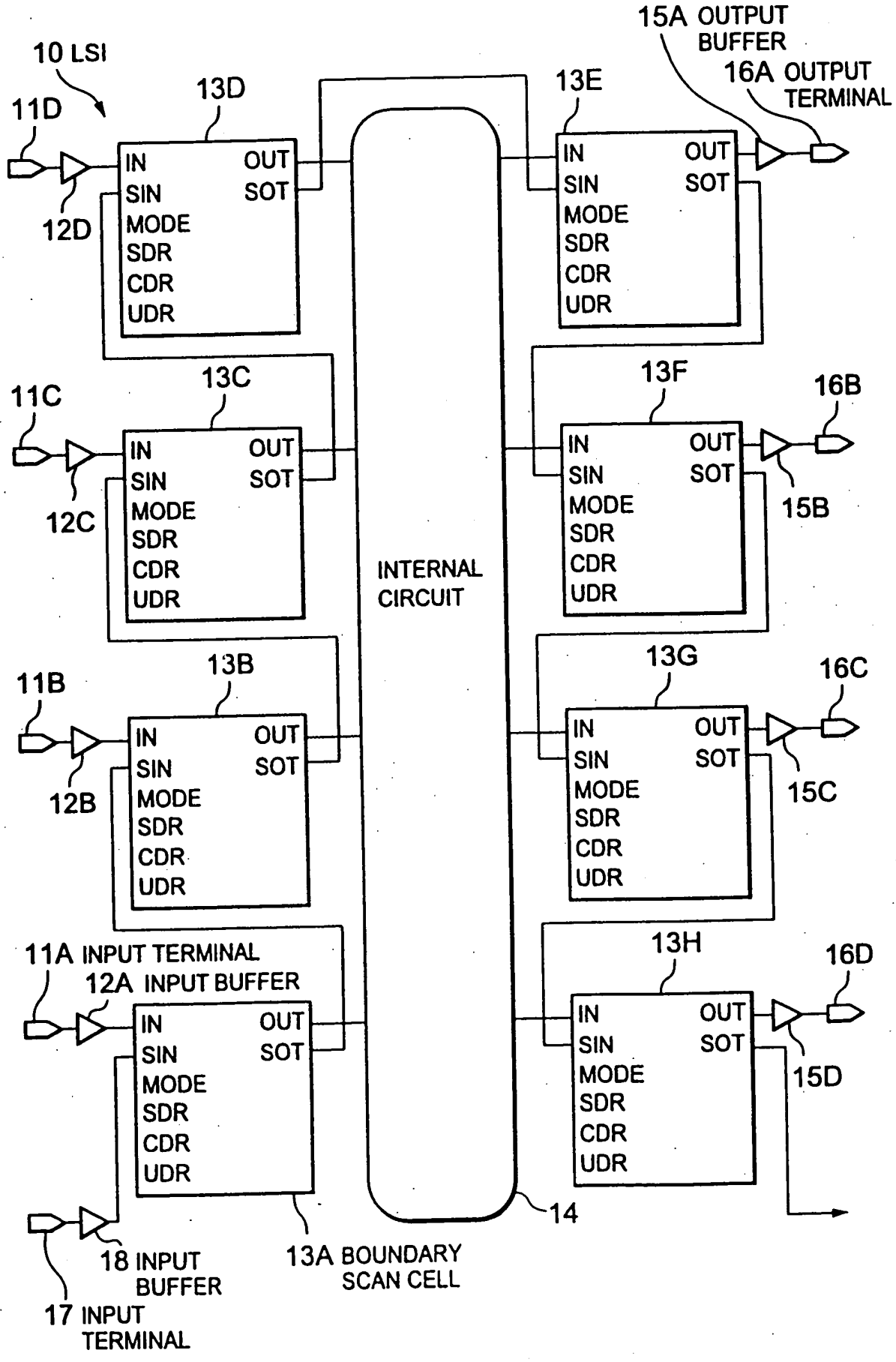
10 LSI
11D
12D
13D
IN
SIN
MODE
SDR
CDR
UDR
OUT
SOT
13E
15A OUTPUT BUFFER
16A OUTPUT TERMINAL
11C
12C
13C
13F
16B
15B
INTERNAL CIRCUIT
11B
12B
13B
13G
16C
15C
11A INPUT TERMINAL
12A INPUT BUFFER
13H
16D
15D
14
18 INPUT BUFFER
17 INPUT TERMINAL
13A BOUNDARY SCAN CELL

FIG.4

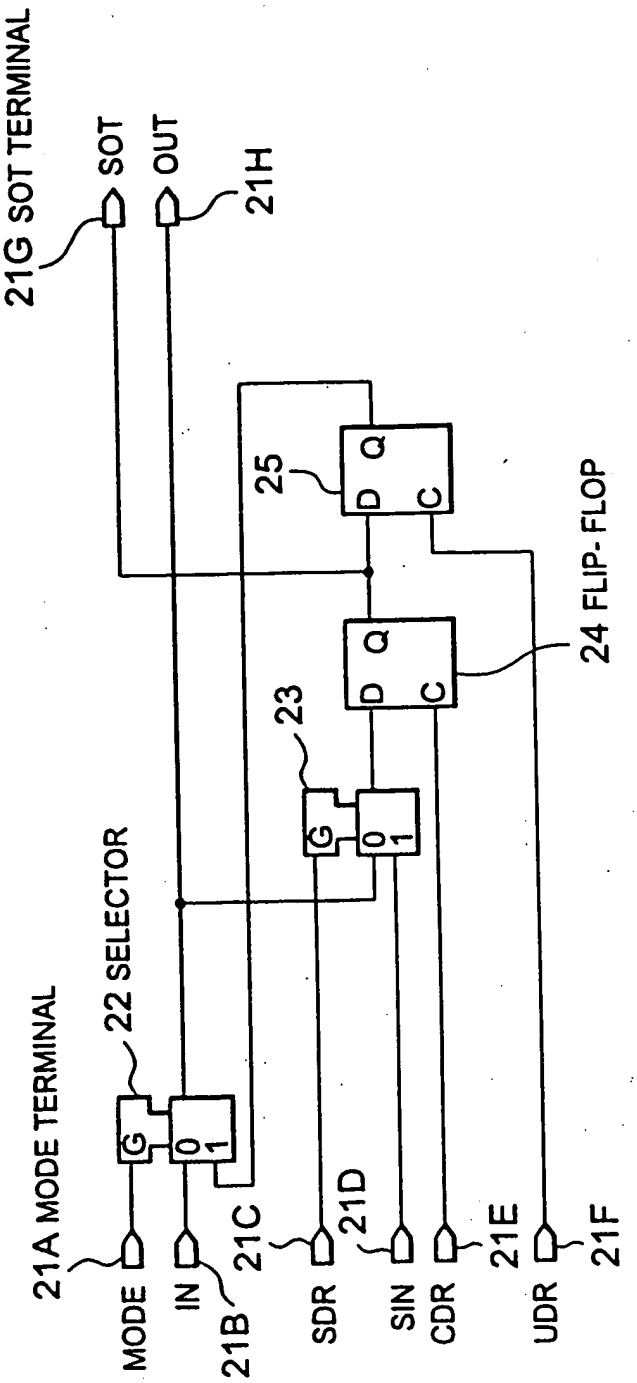
21G SOT TERMINAL
SOT
OUT
21H
25
D
Q
C
24 FLIP- FLOP
23
G
0
1
22 SELECTOR
21A MODE TERMINAL
MODE
IN
21B
21C
SDR
21D
SIN
CDR
21E
UDR
21F

FIG.5

PATTERN NUMBER	OUTPUT TERMINAL 16A	OUTPUT TERMINAL 16B	OUTPUT TERMINAL 16C	OUTPUT TERMINAL 16D
0	0	0	0	0
1	1	1	1	1
2	0	1	0	1

TEST PATTERN

FIG.6

PATTERN NUMBER	OUTPUT TERMINAL 16A	OUTPUT TERMINAL 16B	OUTPUT TERMINAL 16C	OUTPUT TERMINAL 16D
0	0	0	0	0
1-1	1	1	0	0
1-2	1	1	1	1
2	0	1	0	1

TEST PATTERN

TEST PATTERN

FIG.7

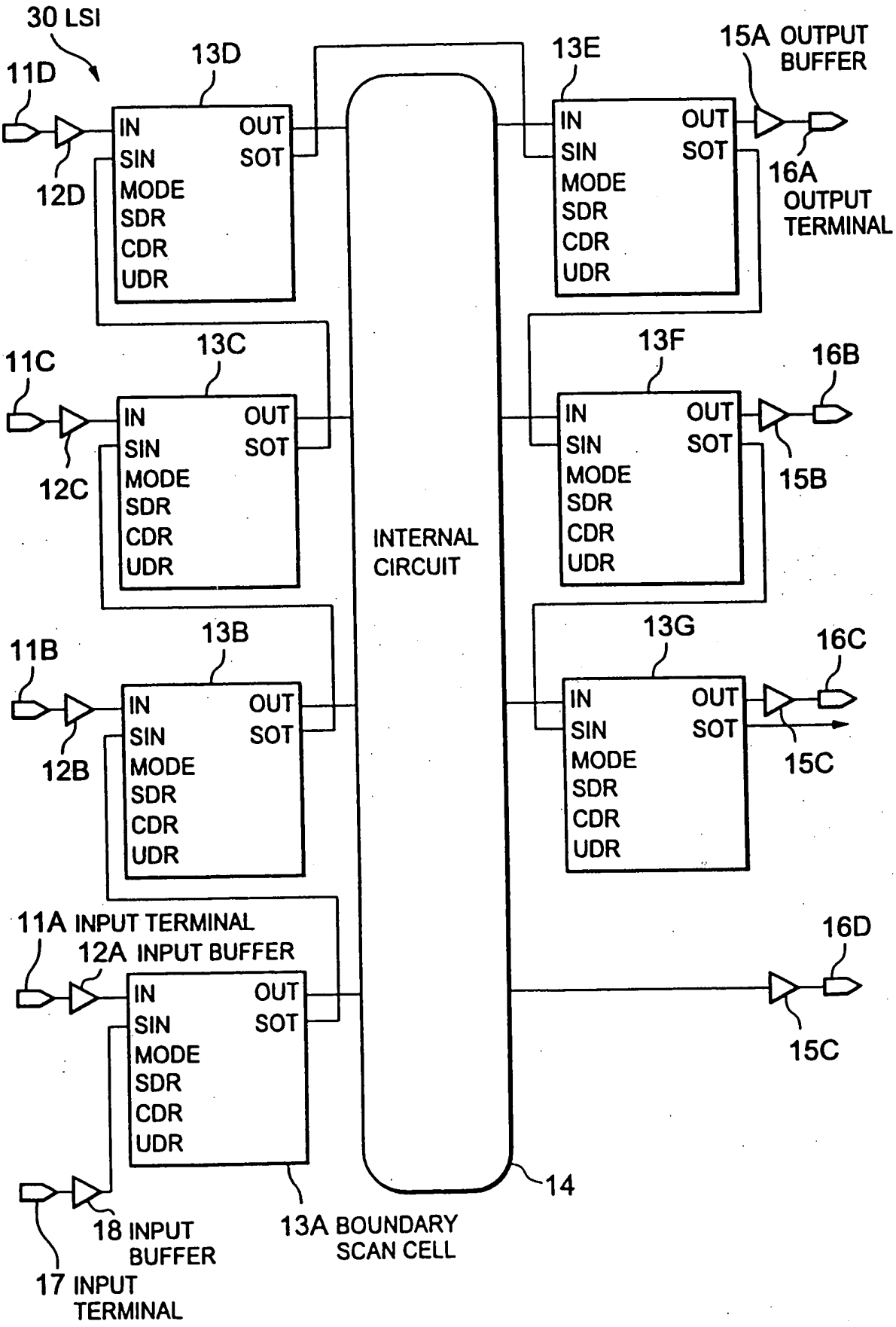
30 LSI
11D
13D
IN
OUT
SIN
SOT
MODE
SDR
CDR
UDR
12D
13E
15A OUTPUT BUFFER
16A OUTPUT TERMINAL
11C
13C
12C
13F
16B
15B
INTERNAL CIRCUIT
11B
13B
12B
13G
16C
15C
11A INPUT TERMINAL
12A INPUT BUFFER
16D
15C
14
18 INPUT BUFFER
13A BOUNDARY SCAN CELL
17 INPUT TERMINAL

FIG.8

PATTERN NUMBER	OUTPUT TERMINAL 16A	OUTPUT TERMINAL 16B	OUTPUT TERMINAL 16C
0	0	0	0
1	1	1	1
2	0	1	0

TEST PATTERN

FIG.9

PATTERN NUMBER	OUTPUT TERMINAL 16A	OUTPUT TERMINAL 16B	OUTPUT TERMINAL 16C
0	0	0	0
1-1	1	0	0
1-2	1	1	0
1-3	1	1	1
2-1	0	1	1
2-1	0	1	0

TEST PATTERN

TEST PATTERN

FIG.10

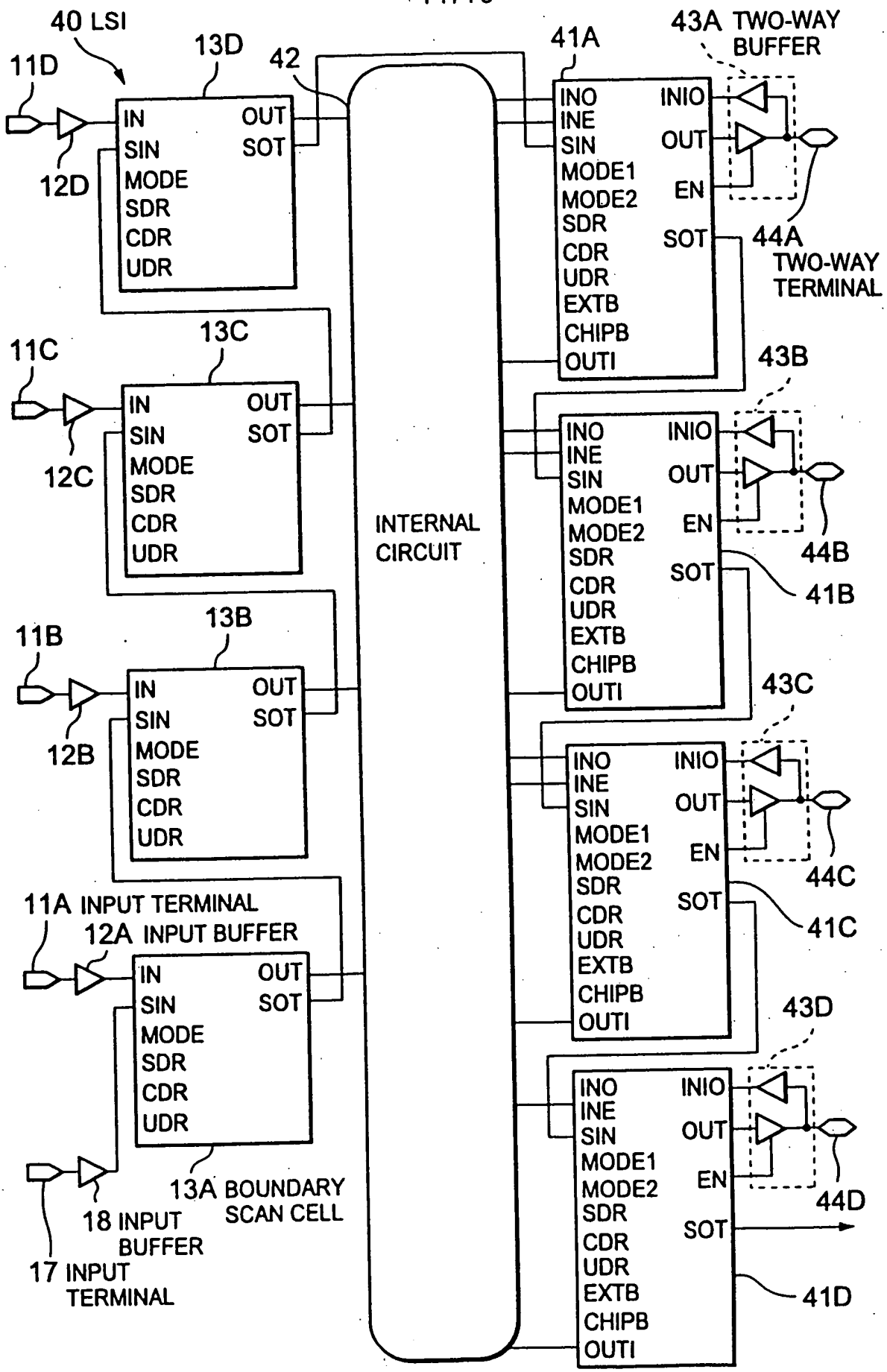
40 LSI
11D
13D
42
41A
43A TWO-WAY BUFFER
12D
IN
SIN
MODE
SDR
CDR
UDR
OUT
SOT
INO
INE
SIN
MODE1
MODE2
SDR
CDR
UDR
EXTB
CHIPB
OUTI
INIO
OUT
EN
SOT
44A TWO-WAY TERMINAL
11C
13C
12C
43B
INTERNAL CIRCUIT
44B
41B
11B
13B
12B
43C
44C
41C
11A INPUT TERMINAL
12A INPUT BUFFER
43D
44D
41D
13A BOUNDARY SCAN CELL
18 INPUT BUFFER
17 INPUT TERMINAL

FIG.11

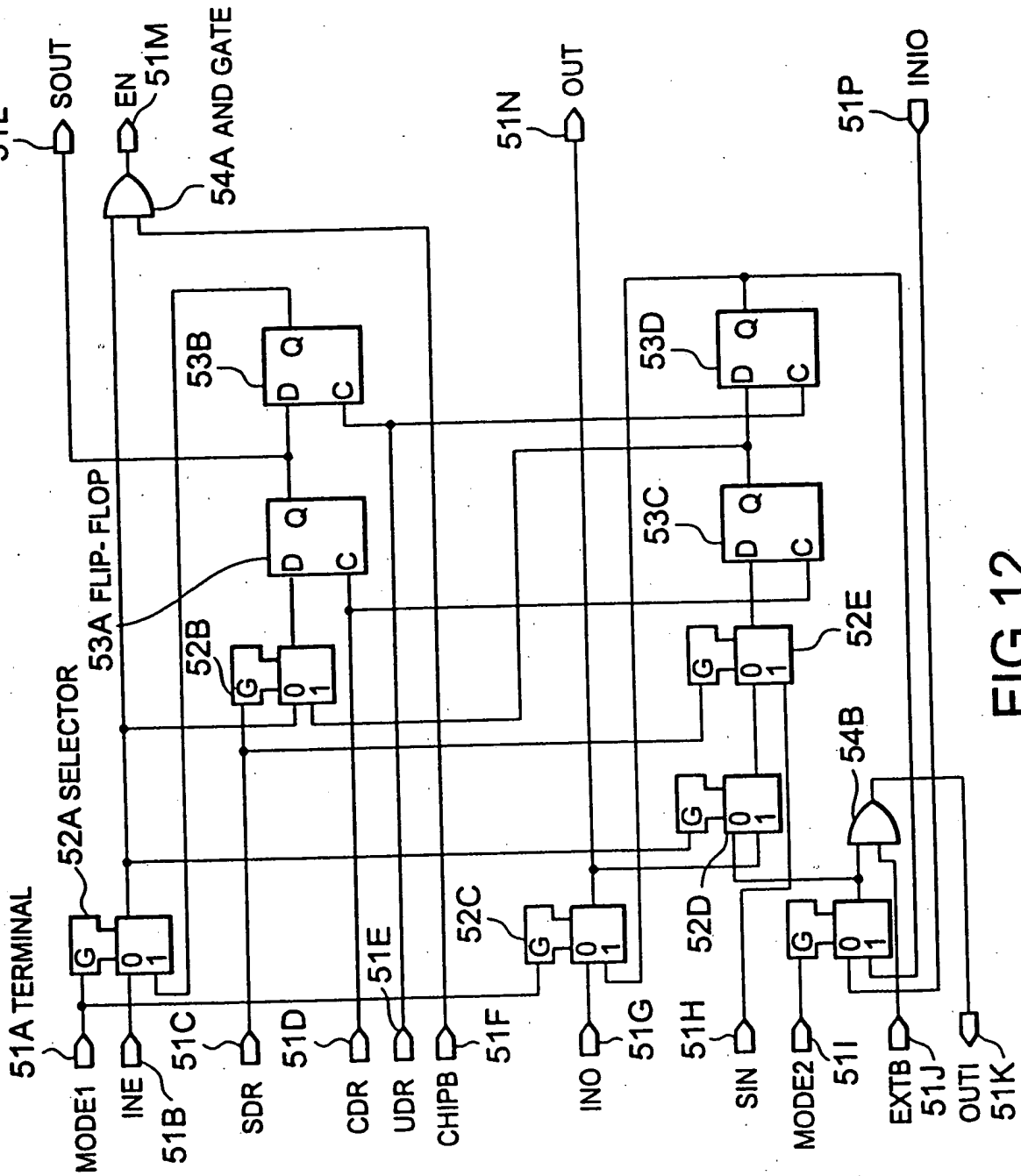
51L
SOUT
EN
51M
54A AND GATE
51N
OUT
51P
INIO
53B
53D
53A FLIP-FLOP
53C
52B
52E
52A SELECTOR
54B
52C
52D
51A TERMINAL
51E
MODE1
INE
51B
51C
SDR
51D
CDR
UDR
CHIPB
51F
INO
51G
51H
SIN
MODE2
51I
EXTB
51J
OUTI
51K

FIG.12

PATTERN NUMBER	OUTPUT EN TERMINAL 44A	OUTPUT EN TERMINAL 44B	OUTPUT EN TERMINAL 44C	OUTPUT EN TERMINAL 44D
0	0	0	0	0
	0	0	0	0
1	1	1	1	1
	0	0	0	0
2	(0)	(0)	(0)	(0)
	1	1	1	1
3	(1)	(1)	(1)	(1)
	1	1	1	1
4	(0)	(1)	(0)	(1)
	1	1	1	1
5	0	0	0	0
	0	0	0	0

0 0 0 0
1 1 1 1
1 0 1 0
TEST PATTERN

FIG.13

PATTERN NUMBER	OUTPUT TERMINAL 44A	EN TERMINAL	OUTPUT TERMINAL 44B	EN TERMINAL	OUTPUT TERMINAL 44C	EN TERMINAL	OUTPUT TERMINAL 44D	EN TERMINAL
0	0	0	0	0	0	0	0	0
1	1	0	1	0	1	0	1	0
2-1	1	1	1	1	1	1	1	1
2-2	0	1	0	1	1	1	1	1
2-3	0	1	0	1	0	1	0	1
3-1	1	1	1	1	0	1	0	1
3-2	1	1	1	1	1	1	1	1
4	0	1	1	1	0	1	1	1
5-1	0	0	1	0	0	0	1	0
5-2	0	0	0	0	0	0	0	0

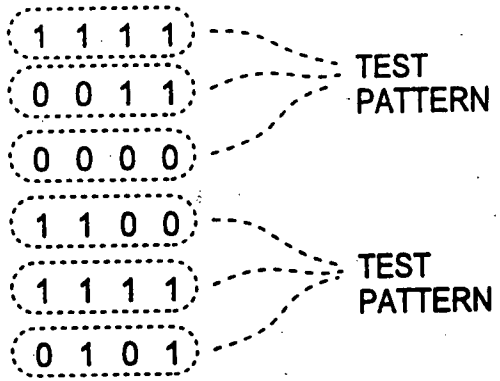

FIG.14

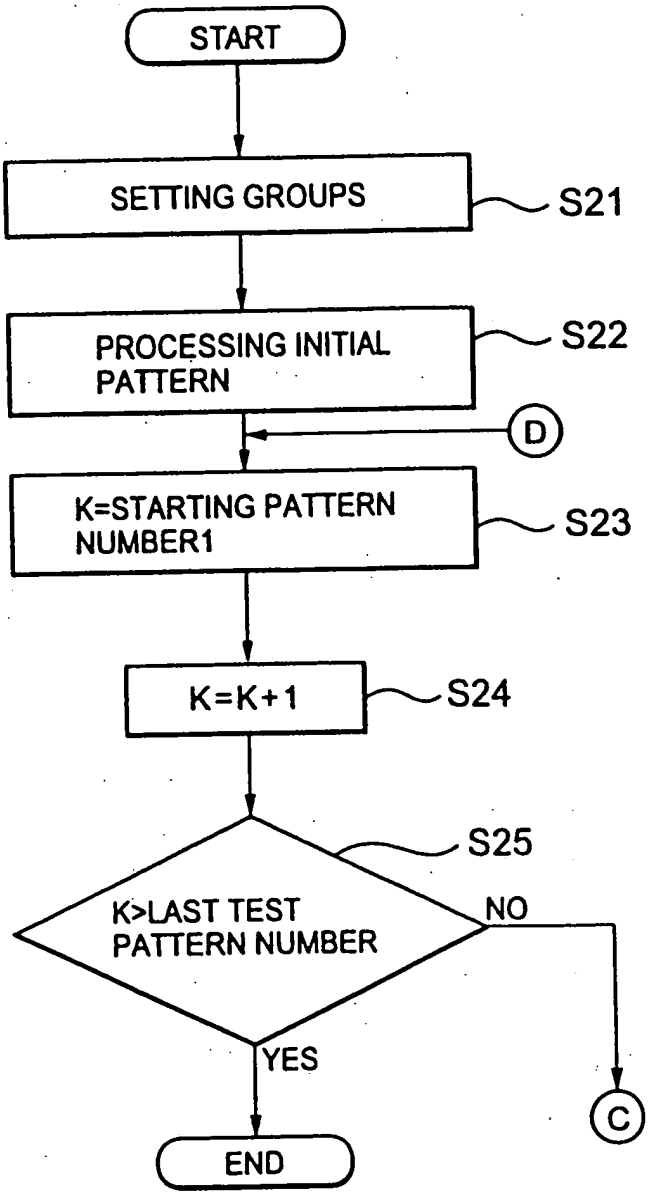
START
SETTING GROUPS
S21
PROCESSING INITIAL PATTERN
S22
D
K=STARTING PATTERN NUMBER1
S23
K=K+1
S24
S25
K>LAST TEST PATTERN NUMBER
NO
YES
C
END

FIG.15

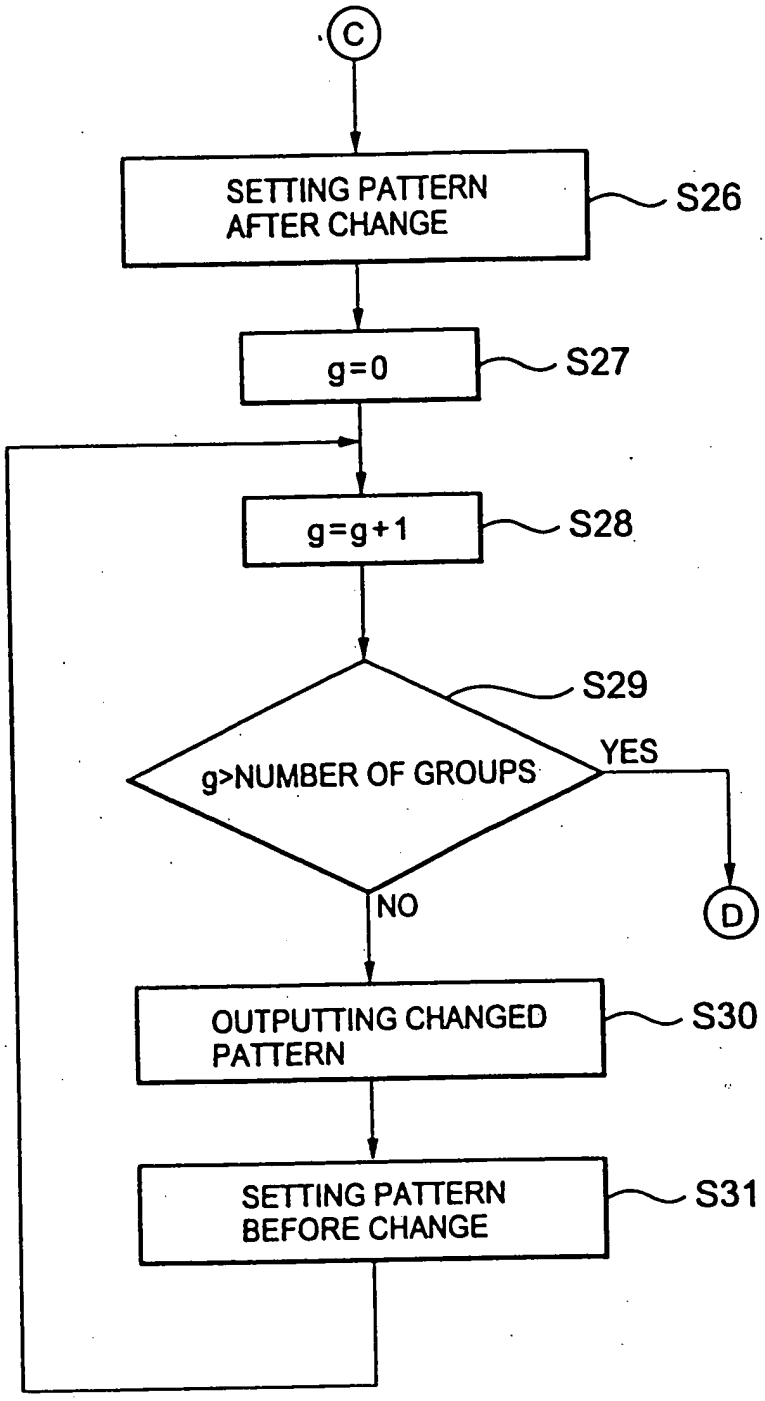
C
SETTING PATTERN AFTER CHANGE
S26
g=0
S27
g=g+1
S28
S29
g>NUMBER OF GROUPS
YES
NO
D
OUTPUTTING CHANGED PATTERN
S30
SETTING PATTERN BEFORE CHANGE
S31

FIG.16

	FIRST GROUP		SECOND GROUP	
PATTERN NUMBER	OUTPUT TERMINAL 16A	OUTPUT TERMINAL 16B	OUTPUT TERMINAL 16C	OUTPUT TERMINAL 16D
0	0	0	0	0
1	1	1	1	1
2	0	1	0	1

FIG.17

	FIRST GROUP		SECOND GROUP	
PATTERN NUMBER	OUTPUT TERMINAL 16A	OUTPUT TERMINAL 16B	OUTPUT TERMINAL 16C	OUTPUT TERMINAL 16D
0	0	0	0	0
2-1	1	1	0	0
2-2	1	1	1	1
3-1	0	1	1	1
3-2	0	1	0	1

FIG.18

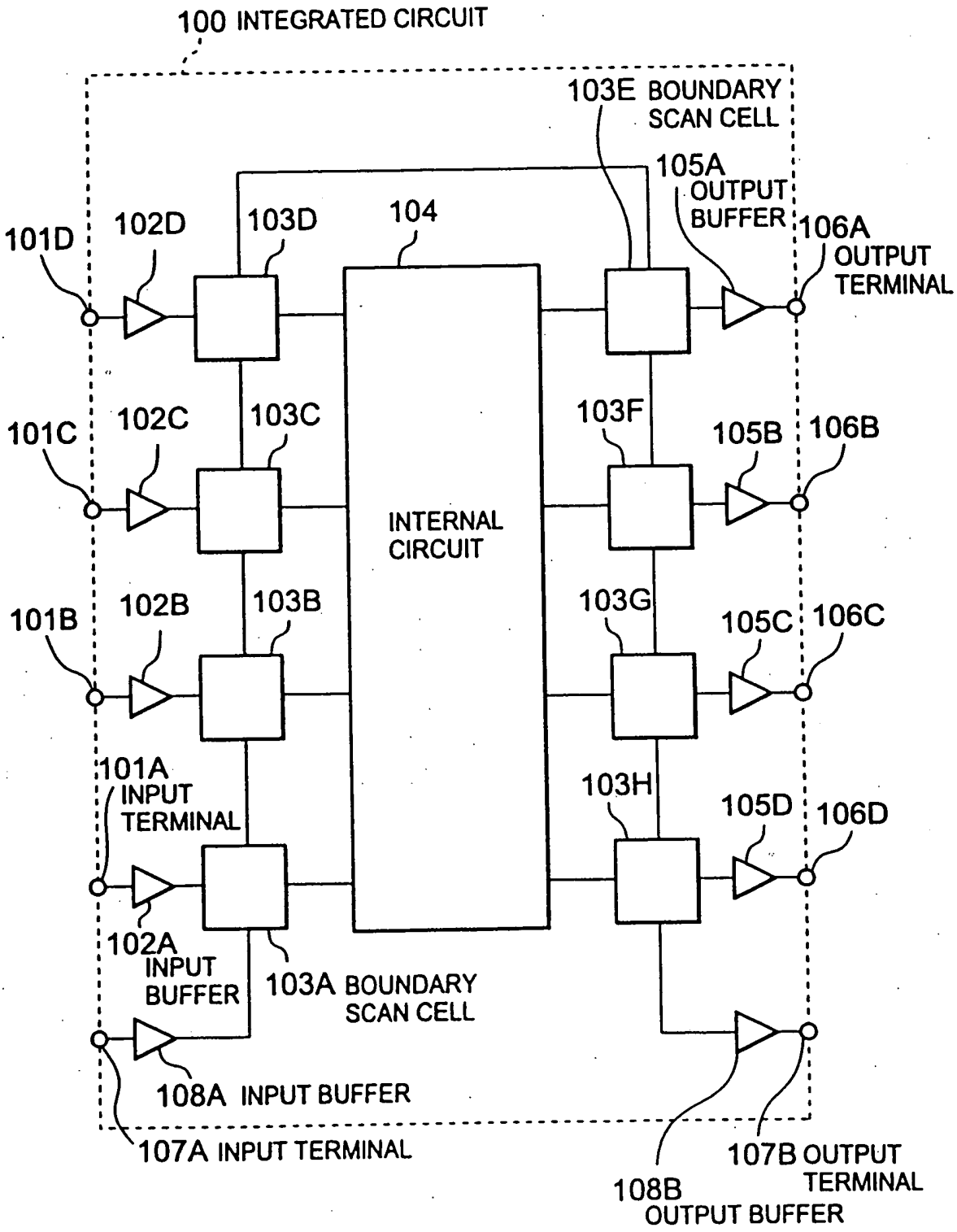
100 INTEGRATED CIRCUIT
103E BOUNDARY SCAN CELL
105A OUTPUT BUFFER
106A OUTPUT TERMINAL
101D
102D
103D
104
101C
102C
103C
103F
105B
106B
INTERNAL CIRCUIT
101B
102B
103B
103G
105C
106C
101A INPUT TERMINAL
103H
105D
106D
102A INPUT BUFFER
103A BOUNDARY SCAN CELL
108A INPUT BUFFER
107A INPUT TERMINAL
108B OUTPUT BUFFER
107B OUTPUT TERMINAL

FIG.19